WBS 1.9 Staged Schedule

Staged DAQ construction plan

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Staged Components

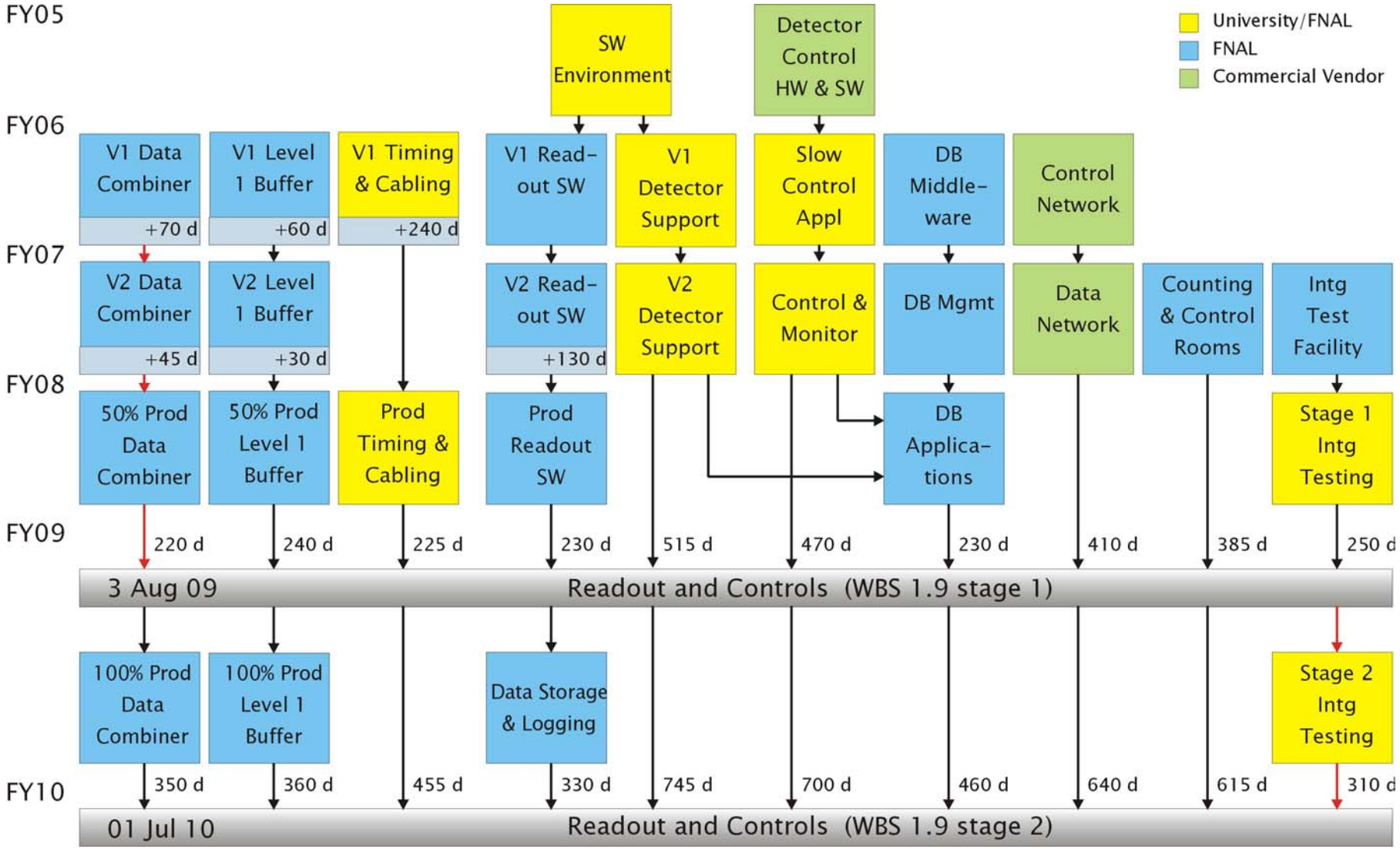
- Stage I – 50% of Readout
  - Needed by August 3, 2009 (Start of shutdown) for DCB installation
  - Ready by September, 2008 (11 months of float)
  - 50% of DCB, L1 buffers, and optical links
  - 100% slow controls, timing hardware
  - Enough of the readout software to support commissioning (mostly done)
  - All database applications with the exception of slow control archiving
- Stage II – 100% of Readout
  - Needed by July 1, 2010 (Start of shutdown) for remaining DCB installation
  - Ready by March, 2009 (15 months of float)
  - 100% of everything
  - Remaining work in FY09 and FY10 is in support of DAQ

What needed to change?

- About a $1M Funding shift from FY09 -> FY08 to purchase electronics in time for the 50% stage.
- Splitting purchase reqs in two large batches (had purchased complete quantities before) for DCBs, L1 buffers, and optical links.
- Minor shuffling of quantities with large floats to try and stay on track in other areas in funding profile (not much happening in FY05).

	FY05	**FY06**	**FY07**	**FY08**	**FY09**	**FY10**
CD-1	393K	2,669K	3,571K	5,090K	4,614K	
Staged	436K	2,662K	3,624K	5,955K	3,598K	109K
Net Change	43K	(7K)	53K	865K	(1016K)	109K

WBS 1.9 Project Flow Diagram



Critical path

- Stage I
  - several paths ending within 30 days
  - Most have inherent catchup periods at each fiscal year while waiting for next fiscal year's funding.
- Stage II
  - Integration
  - Purchasing/commissioning mass storage system. Want to delay purchase in FY06 to get biggest bang for the buck.

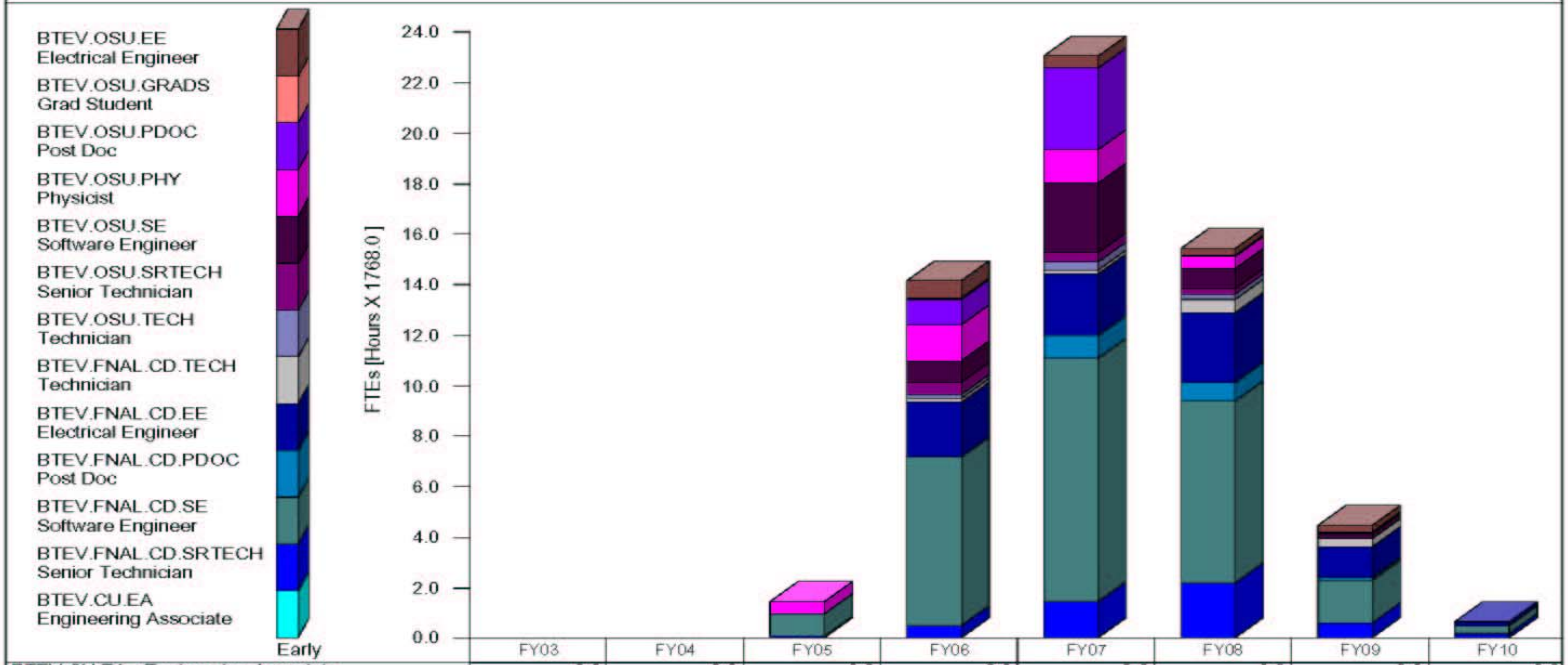
WBS 1.9 Labor profile

BTeV - WBS 1.9 Event Readout and Controls Electronics and Software

Construction Labor Time Profile (FTEs) by Fiscal Year

BTeV FTE Labor

20May04



	FY03	FY04	FY05	FY06	FY07	FY08	FY09	FY10
BTEV.CU.EA : Engineering Associate	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
BTEV.FNAL.CD.SRTECH : Senior Technician	0.0	0.0	0.0	0.5	1.4	2.1	0.6	0.1
BTEV.FNAL.CD.SE : Software Engineer	0.0	0.0	0.9	6.7	9.7	7.2	1.7	0.3
BTEV.FNAL.CD.PDOC : Post Doc	0.0	0.0	0.0	0.0	0.9	0.7	0.1	0.0
BTEV.FNAL.CD.EE : Electrical Engineer	0.0	0.0	0.0	2.2	2.4	2.8	1.2	0.1
BTEV.FNAL.CD.TECH : Technician	0.0	0.0	0.0	0.2	0.2	0.5	0.3	0.0
BTEV.OSU.TECH : Technician	0.0	0.0	0.0	0.1	0.3	0.2	0.0	0.0
BTEV.OSU.SRTECH : Senior Technician	0.0	0.0	0.0	0.5	0.4	0.2	0.0	0.0
BTEV.OSU.SE : Software Engineer	0.0	0.0	0.0	0.9	2.7	0.8	0.2	0.0
BTEV.OSU.PHY : Physicist	0.0	0.0	0.5	1.4	1.4	0.5	0.0	0.0
BTEV.OSU.PDOC : Post Doc	0.0	0.0	0.0	1.0	3.2	0.1	0.0	0.0
BTEV.OSU.GRADS : Grad Student	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
BTEV.OSU.EE : Electrical Engineer	0.0	0.0	0.0	0.7	0.5	0.3	0.2	0.0

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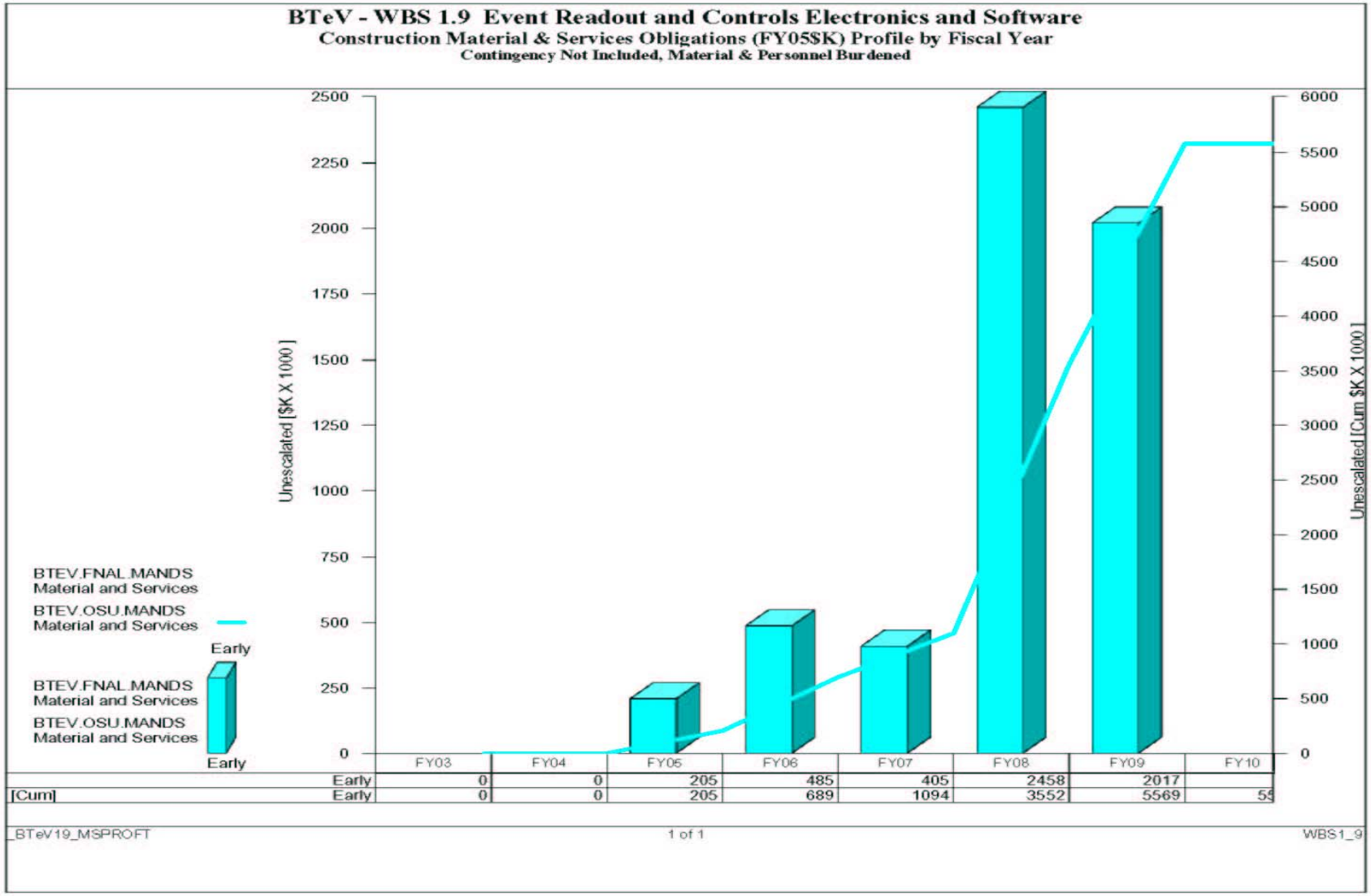
WBS 1.9 Cost profile



CD-1 Recommendations (1.8 and 1.9)

- Daq ready 6-9 months before first beam
  - Done (and then some!)
- FPGA de-escalation too aggressive
  - Will do, but we believe will be no significant cost change. We can balance between increase in performance and price decreasing.
- Assign [physicist] staffing.
  - Primarily 1.8 issue.